

2116  
PTO/SB/21 (08-03)

<b>TRANSMITTAL FORM</b> (to be used for all correspondence after initial filing)		Application Number	09/880,734
		Filing Date	June 12, 2001
		First Named Inventor	Crosland, Andrew
		Art Unit	2116
		Examiner Name	Tse W. Chen
Total Number of Pages in This Submission *6 IDS References	5 and *	Attorney Docket Number	15114-053500US

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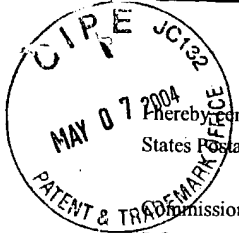
ENCLOSURES (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual	Townsend and Townsend and Crew LLP Melvin D. Chan Reg. No. 39,626
Signature	
Date	May 5, 2004

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By:

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In re application of:

ANDREW CROSLAND et al.

Application No.: 09/880,734

Filed: June 12, 2001

For: EMBEDDED PROCESSOR WITH  
WATCHDOG TIMER FOR  
PROGRAMMABLE LOGIC

Examiner: Tse W. Chen

Art Unit: 2116

SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT UNDER 37  
CFR §1.97 and §1.98

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

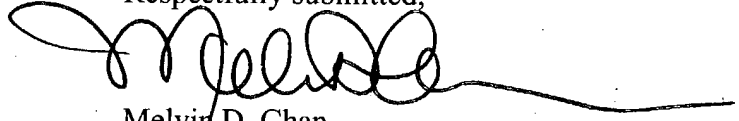
As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

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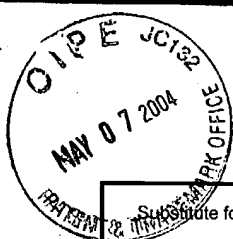
Respectfully submitted,



Melvin D. Chan  
Reg. No. 39,626

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PTO/SB/08A (08-03)

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Substitute for form 1449A/PTO			
		<b>Complete if Known</b>			
		Application Number	09/880,734		
		Filing Date	June 12, 2001		
		First Named Inventor	Crosland, Andrew		
		Art Unit	2116		
Sheet	1	of	2	Examiner Name	Tse W. Chen
				Attorney Docket Number	15114-053500US

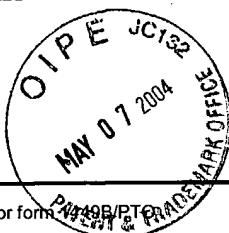
U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <sup>2</sup> (if known)			
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FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	7 <sup>6</sup>
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	09/880,734
				Filing Date	June 12, 2001
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				Art Unit	2116
				Examiner Name	Tse W. Chen
Sheet	2	of	2	Attorney Docket Number	15114-053500US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AO	DeHON, DPGA-Coupled Microprocessors: Commodity ICs for the Early 21st Century, Artificial Intelligence Laboratory, Massachusetts Institute of Technology, Cambridge, MA, IEEE, February, 1994, pp. 31-33	
	AP	HAUSER, and WAWRZYNEK, University of California, Berkeley, "Garp: A MIPS Processor with a Reconfigurable Coprocessor," IEEE, April 1997, pp. 12-21.	
	AQ	IBM Corporation, "Mixture of Field and Factory Programmed Logic Cells in a Single Device," IBM Technical Disclosure Bulletin, April 1995, pp. 499-500	
	AR	NAGEL, "ACM Computing Surveys: Synergy Between Software and Hardware," Carnegie Mellon University, Department of Electrical Engineering and Computer Science, Pittsburgh, PA, December, 1996, pp. 1-3.	
	AS	RAZDAN, and SMITH, "A High-Performance Microarchitecture with Hardware-Programmable Functional Units," Harvard University, Cambridge, MA, Digital Equipment Corporation, Hudson, MA, November, 1994, pp. 172-180.	
	AT	WITTIG, and CHOW, "OneChip" An FPGA Processor With Reconfigurable Logic," Department of Electrical and Computer Engineering, University of Toronto, Ontario, Canada, IEEE, September, 1996, pp. 126-135.	
	AU	WYNN, "In-Circuit Emulation for ASIC-Based Designs," Xilinx, Inc., VLSI Systems Design, October, 1986, pp. 38-39, and 42-45.	
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